IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s): Daniel John Devine and David Thompson
Case: 2
Serial No.: 10/787,376
Filing Date: February 26, 2004
Examiner: 2182
Group: Jasjit S. Vidwan

Title: Controller for Peripheral Communications with Processing Capacity for Peripheral Functions

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DECLARATION OF KEVIN M. MASON

I, the undersigned, hereby declare and state as follows:

1. I am an attorney in the firm of Ryan, Mason, & Lewis, LLP; I am an attorney of record in the above-identified case; and I drafted the patent application for the above-identified case.

2. Prior to May 13, 2003, an Agere System Requirements Document, entitled "USS2827 USB 2.0 Device Controller" was prepared by the inventors of the above-identified case. A copy of the Requirements Document is attached hereto as Exhibit 2.

3. On or about July 11, 2003, the Invention Submission document, subsequently assigned Submission No. 124809, entitled "ARM7 Processor based USB 2.0 Device Controller," was submitted to a former Agere in-house patent attorney, Robert P. Marley. The date that the Invention Submission document was Received by Agere IP Law is noted in the upper right hand portion of the document as July 11, 2003. A copy of the Invention Submission document dated July 11, 2003 is attached hereto as Exhibit 5.

4. In accordance with the standard practices of Agere, the Invention Submission document was queued for review by the former in-house patent attorney, Robert P. Marley. Mr. Marley subsequently reviewed the Invention Submission and presented it for an internal review by the Agere Systems Patent Committee on or about August 13, 2003.

5. On or about September 10, 2003, the Agere Systems Patent Committee approved the assignment of the patent application to Ryan, Mason & Lewis, LLP ("RML").

6. The Requirements Document and the Invention Submission document describe an invention falling within one or more of the claims of the present application. For example, Applicants note that pending claims 4, 5, 10, 11, 17, and 18 are supported by FIG. 3 and the corresponding discussion of the present application (This figure appears on page 4 of the Requirements Document). Exhibits 2 and 5 provide evidence that the aspects of the invention claimed in claims 4, 5, 10, 11, 17, and 18 and supported by FIG. 3 were conceived on or before May 13, 2003.

7. On October 15, 2003, a letter was sent to Ryan, Mason & Lewis, LLP requesting that the patent application be prepared and filed. A copy of the letter dated October 15, 2003 is attached hereto as Exhibit 6. RML subsequently accepted the patent application request and, in standard practice with RML, assigned the application to me.

8. During the period of October 18-21, 2003, RML circulated among all RML attorneys and Patent Agents a "New Matters Conflict List" that included the above-identified patent application. A copy of the "New Matters Conflict List" is attached hereto as Exhibit A.

9. On October 20, 2003, I sent Mr. Devine a message via electronic mail introducing myself as the attorney handling preparation of the above-identified patent application. As indicated in the message, I estimated that I would begin actively working on the application in late November, 2003, due to my caseload at that time. A copy of the electronic mail message is attached hereto as Exhibit B.

10. During the period from prior to October 20, 2003 until January 12, 2004, I was responsible for a large number of unrelated cases and it was my general practice to arrange initial evaluation meetings with inventors substantially in the order in which the computerized invention disclosure documents were received in the system.

11. During the period from prior to October 20, 2003 until January 12, 2004, I reviewed the Requirements Document and Invention Submission document and requested a meeting with Mr. Daniel Devine, a co-inventor of the above-referenced application.

12. On or about January 12, 2004, Mr. Daniel Devine and I met to discuss the above-referenced application. A copy of an electronic mail message from Mr. Devine to me documenting this meeting is attached hereto as Exhibit 7.

13. I studied the Invention Submission document and notes from the meeting on or about January 12, 2004 and started preparation of the patent application.

14. On or about February 3, 2004, Mr. Devine provided electronic copies of the disclosure material via electronic mail to me. A copy of an electronic mail message from Mr. Devine to me documenting this exchange is attached hereto as Exhibit 8.

15. On or about February 5, 2004, I sent a first draft of the present application via electronic mail to Mr. Devine. A copy of an electronic mail message to Mr. Devine documenting this exchange is included in the email history shown in Exhibit 9.

16. Mr. Devine reviewed the application and met with a co-inventor to receive additional comments.

17. On or about February 23, 2004, Mr. Devine approved the draft application. A copy of an electronic mail message from Mr. Devine to me containing this approval is included in the email history shown in Exhibit 9.

18. I sent a final draft via electronic mail to Mr. Devine on February 23, 2004. A copy of an electronic mail message to Mr. Devine documenting this exchange is included in the email history shown in Exhibit 9.

19. The final draft was approved by Mr. Devine on February 23, 2004. A copy of an electronic mail message from Mr. Devine to me documenting this approval is included in the email history shown in Exhibit 9.

20. As noted above, the present patent application was filed by Mr. Mason on February 26, 2004.

21. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

22. I understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and may jeopardize the validity of the application or any patent issuing thereon.

Date: 6/23/09

Kevin M. Mason

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

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DECLARATION UNDER 37 C.F.R. §1.131

We, the undersigned, hereby declare and state as follows:

1. We are named joint inventors of the invention that is the subject of the above-referenced U.S. patent application. We have assigned our respective interests in the patent application to Agere Systems Inc. ("Agere").

2. The invention was conceived on or before May 13, 2003 and all inventive activity described herein took place in the United States of America.

3. A draft of a presentation entitled "Wired Product Line USB/1394 Product Family" is attached hereto as Exhibit 1. Sheet 16 of the presentation shows a product roadmap including the USS2827 - USB 2.0 Device Controller which is a USB 2.0 device controller incorporating the ARM processor described in the above-identified application. Certain information has been redacted from Exhibit 1. The creation date of the presentation is May 2, 2003, as evidenced by the screenshot attached hereto as Exhibit 1A.

4. Prior to May 13, 2003, we prepared an Agere System Requirements Document, entitled "USS2827 USB 2.0 Device Controller." A copy of the Requirements Document is attached hereto as Exhibit 2.

5. During the period of May 13, 2003, to July 11, 2003, we diligently worked on the invention of the above-identified patent application and exchanged a continuous stream of electronic mail messages with colleagues regarding the invention, as evidenced by a transcript of the electronic mail messages. A copy of the electronic mail transcript is attached hereto as Exhibit 3. Certain information has been redacted from Exhibit 3.

6. On May 27, 2003, Mr. Prasad, an employee of Agere, sent a note via electronic mail to David Thompson and Sherre Staves with queries related to the "USS2827 USB 2.0 Device Controller." A copy of the electronic mail from Mr. Prasad is attached hereto as Exhibit 4.

7. During the months of June and July, 2003, we prepared an Invention Submission document as required by Agere.

8. On or about July 11, 2003, the Invention Submission document, subsequently assigned Submission No. 124809, entitled "ARM7 Processor based USB 2.0 Device Controller," was submitted to a former Agere in-house patent attorney, Robert P. Marley. The date that the Invention Submission document was Received by Agere IP Law is noted in the upper right hand portion of the document as July 11, 2003. A copy of the Invention Submission document dated July 11, 2003 is attached hereto as Exhibit 5.

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13. Mr. Kevin Mason subsequently reviewed the Requirements Document and Invention Submission document and requested a meeting with Mr. Daniel Devine, a co-inventor of the above-referenced application.

10. On or about January 12, 2004, Mr. Kevin Mason and Mr. Daniel Devine met to discuss the above-referenced application. A copy of an electronic mail message from Mr. Devine to Mr. Mason documenting this meeting is attached hereto as Exhibit 7.

11. Mr. Mason studied the Invention Submission document and notes from the meeting on or about January 12, 2004 and started preparation of the patent application.

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20. We understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing thereon.

Date: 6/22/09

Daniel John Devine

Date: 6/22/09

David Thompson

Exh. 1

dbrass:

Dan to do this section

Wired Product Line
USB/1394 Product Family

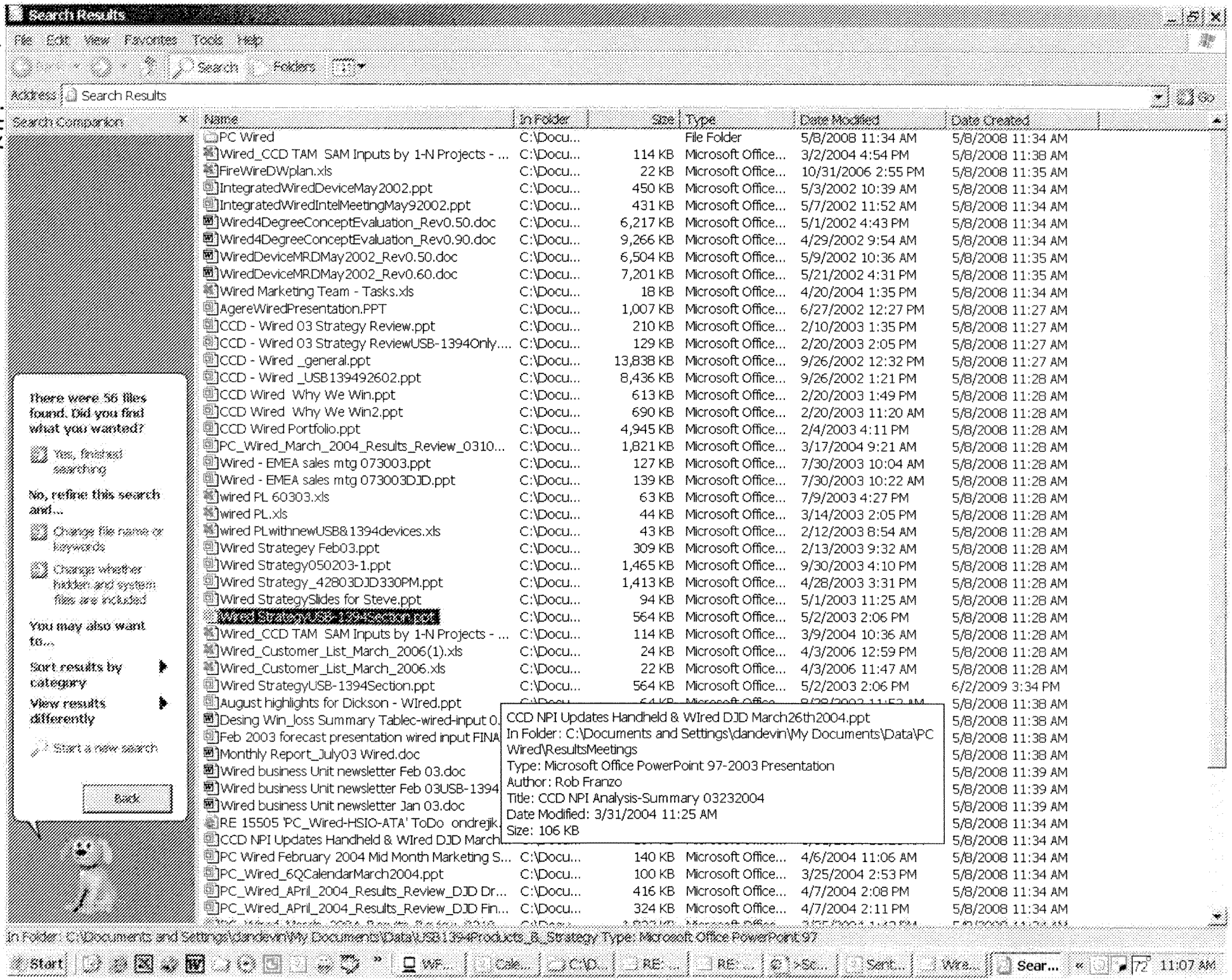
agere systems

Key Messages & Business Model Assumptions

- **Objective: Minimum investment scenario for sustaining current revenue and maintaining viable market presence**
  - **Continue marketing current products:**
  - **We will leverage existing IP/Partnerships for increasing product breadth and depth:**
    - **Examples:**
      - **1394B Phy – 3rd party private label**
        - **Improves product breadth**
      - **USS2827 – USB 2.0 Device Controller**
        - **USB 2.0 Soft Modem**
        - **USB 2.0 Peripherals**

- **Business Model Assumptions:**
  - **Market momentum in USB and 1394 continues and all indications are that it will**
  - **Product Line can be augmented by external 3rd parties for low-risk, fast time-to-market revenue**

Exh. 1A


Search Results
File Edit View Favorites Tools Help
Search Folders
Address Search Results
Go
Search Companion
There were 56 files found. Did you find what you wanted?
Yes, finished searching
No, refine this search and...
Change file name or keywords
Change whether hidden and system files are included
You may also want to...
Sort results by category
View results differently
Start a new search
Back
Name | In Folder | Size | Type | Date Modified | Date Created
PC Wired C:\Docu... File Folder 5/8/2008 11:34 AM 5/8/2008 11:34 AM
Wired_CCD TAM SAM Inputs by 1-N Projects - ... C:\Docu... 114 KB Microsoft Office... 3/2/2004 4:54 PM 5/8/2008 11:38 AM
FireWireDWplan.xls C:\Docu... 22 KB Microsoft Office... 10/31/2006 2:55 PM 5/8/2008 11:35 AM
IntegratedWiredDeviceMay2002.ppt C:\Docu... 450 KB Microsoft Office... 5/3/2002 10:39 AM 5/8/2008 11:34 AM
IntegratedWiredIntelMeetingMay92002.ppt C:\Docu... 431 KB Microsoft Office... 5/7/2002 11:52 AM 5/8/2008 11:34 AM
Wired4DegreeConceptEvaluation_Rev0.50.doc C:\Docu... 6,217 KB Microsoft Office... 5/1/2002 4:43 PM 5/8/2008 11:34 AM
Wired4DegreeConceptEvaluation_Rev0.90.doc C:\Docu... 9,266 KB Microsoft Office... 4/29/2002 9:54 AM 5/8/2008 11:34 AM
WiredDeviceMRDMay2002_Rev0.50.doc C:\Docu... 6,504 KB Microsoft Office... 5/9/2002 10:36 AM 5/8/2008 11:35 AM
WiredDeviceMRDMay2002_Rev0.60.doc C:\Docu... 7,201 KB Microsoft Office... 5/21/2002 4:31 PM 5/8/2008 11:35 AM
Wired Marketing Team - Tasks.xls C:\Docu... 18 KB Microsoft Office... 4/20/2004 1:35 PM 5/8/2008 11:34 AM
AgereWiredPresentation.PPT C:\Docu... 1,007 KB Microsoft Office... 6/27/2002 12:27 PM 5/8/2008 11:27 AM
CCD - Wired 03 Strategy Review.ppt C:\Docu... 210 KB Microsoft Office... 2/10/2003 1:35 PM 5/8/2008 11:27 AM
CCD - Wired 03 Strategy ReviewUSB-1394Only.... C:\Docu... 129 KB Microsoft Office... 2/20/2003 2:05 PM 5/8/2008 11:27 AM
CCD - Wired _general.ppt C:\Docu... 13,838 KB Microsoft Office... 9/26/2002 12:32 PM 5/8/2008 11:27 AM
CCD - Wired _USB139492602.ppt C:\Docu... 8,436 KB Microsoft Office... 9/26/2002 1:21 PM 5/8/2008 11:28 AM
CCD Wired Why We Win.ppt C:\Docu... 613 KB Microsoft Office... 2/20/2003 1:49 PM 5/8/2008 11:28 AM
CCD Wired Why We Win2.ppt C:\Docu... 690 KB Microsoft Office... 2/20/2003 11:20 AM 5/8/2008 11:28 AM
CCD Wired Portfolio.ppt C:\Docu... 4,945 KB Microsoft Office... 2/4/2003 4:11 PM 5/8/2008 11:28 AM
PC_Wired_March_2004_Results_Review_0310... C:\Docu... 1,821 KB Microsoft Office... 3/17/2004 9:21 AM 5/8/2008 11:28 AM
Wired - EMEA sales mtg 073003.ppt C:\Docu... 127 KB Microsoft Office... 7/30/2003 10:04 AM 5/8/2008 11:28 AM
Wired - EMEA sales mtg 073003DJD.ppt C:\Docu... 139 KB Microsoft Office... 7/30/2003 10:22 AM 5/8/2008 11:28 AM
wired PL 60303.xls C:\Docu... 63 KB Microsoft Office... 7/9/2003 4:27 PM 5/8/2008 11:28 AM
wired PL.xls C:\Docu... 44 KB Microsoft Office... 3/14/2003 2:05 PM 5/8/2008 11:28 AM
wired PLwithnewUSB&1394devices.xls C:\Docu... 43 KB Microsoft Office... 2/12/2003 8:54 AM 5/8/2008 11:28 AM
Wired Strategey Feb03.ppt C:\Docu... 309 KB Microsoft Office... 2/13/2003 9:32 AM 5/8/2008 11:28 AM
Wired Strategy050203-1.ppt C:\Docu... 1,465 KB Microsoft Office... 9/30/2003 4:10 PM 5/8/2008 11:28 AM
Wired Strategy_42803DJD330PM.ppt C:\Docu... 1,413 KB Microsoft Office... 4/28/2003 3:31 PM 5/8/2008 11:28 AM
Wired StrategySlides for Steve.ppt C:\Docu... 94 KB Microsoft Office... 5/1/2003 11:25 AM 5/8/2008 11:28 AM
Wired StrategyUSB-1394Section.ppt C:\Docu... 564 KB Microsoft Office... 5/2/2003 2:06 PM 5/8/2008 11:28 AM
Wired_CCD TAM SAM Inputs by 1-N Projects - ... C:\Docu... 114 KB Microsoft Office... 3/9/2004 10:36 AM 5/8/2008 11:28 AM
Wired_Customer_List_March_2006(1).xls C:\Docu... 24 KB Microsoft Office... 4/3/2006 12:59 PM 5/8/2008 11:28 AM
Wired_Customer_List_March_2006.xls C:\Docu... 22 KB Microsoft Office... 4/3/2006 11:47 AM 5/8/2008 11:28 AM
Wired StrategyUSB-1394Section.ppt C:\Docu... 564 KB Microsoft Office... 5/2/2003 2:06 PM 6/2/2009 3:34 PM
August highlights for Dickson - WIred.ppt 5/8/2008 11:38 AM
Desing Win_loss Summary Tablec-wired-input 0... 5/8/2008 11:38 AM
Feb 2003 forecast presentation wired input FINA... 5/8/2008 11:38 AM
Monthly Report_July03 Wired.doc 5/8/2008 11:38 AM
Wired business Unit newsletter Feb 03.doc 5/8/2008 11:39 AM
Wired business Unit newsletter Feb 03USB-1394... 5/8/2008 11:39 AM
Wired business Unit newsletter Jan 03.doc 5/8/2008 11:39 AM
RE 15505 'PC_Wired-HSIO-ATA' ToDo ondrejk... 5/8/2008 11:34 AM
CCD NPI Updates Handheld & WIred DJD March... 5/8/2008 11:34 AM
PC Wired February 2004 Mid Month Marketing S... C:\Docu... 140 KB Microsoft Office... 4/6/2004 11:06 AM 5/8/2008 11:34 AM
PC_Wired_6QCalendarMarch2004.ppt C:\Docu... 100 KB Microsoft Office... 3/25/2004 2:53 PM 5/8/2008 11:34 AM
PC_Wired_APril_2004_Results_Review_DJD Dr... C:\Docu... 416 KB Microsoft Office... 4/7/2004 2:08 PM 5/8/2008 11:34 AM
PC_Wired_APril_2004_Results_Review_DJD Fin... C:\Docu... 324 KB Microsoft Office... 4/7/2004 2:11 PM 5/8/2008 11:34 AM
CCD NPI Updates Handheld & WIred DJD March26th2004.ppt
In Folder: C:\Documents and Settings\dandevin\My Documents\Data\PC Wired\ResultsMeetings
Type: Microsoft Office PowerPoint 97-2003 Presentation
Author: Rob Franzo
Title: CCD NPI Analysis-Summary 03232004
Date Modified: 3/31/2004 11:25 AM
Size: 106 KB
In Folder: C:\Documents and Settings\dandevin\My Documents\Data\USB1394Products_&_Strategy Type: Microsoft Office PowerPoint 97
Start
Sear...
11:07 AM

Exh. 2

May 13, 2003

agere systems

USS2827 USB 2.0 Device Controller System Requirements Document

Table of Contents

Introduction

This document defines the requirements of the USS2827 device controller from a system perspective. There is enough detail about the achitecture and interfaces of the device to allow the various development disciplines to begin estimating the effort involved in creating such a device. Some areas will require more detailed specification before actual design begins.

The USS2827 Marketing Requirements Document describes the intended markets for this device and should be used as a reference.

Features

- Integrated ARM7TDMI core operating at up to 120 MHz
- Integrated USB 2.0 device controller.
  - USB revision 2.0 and 1.1 compliant.
  - Self-powered or bus-powered USB device.
  - 2K USB FIFOs.
  - Supports up to 16 USB endpoints.
  - Supports control, interrupt, bulk, and isochronous transfers for all 16 endpoints.
  - Supports USB remote wake-up feature.
  - Integrated USB transceivers for high-speed, full-speed, and low-speed operation
  - 5 V tolerant I/O buffers allow operation in 3 V or 5 V environments.
- 4K x 32 on-chip ROM for code storage.
- 2K x 32 on-chip RAM.
- On-chip PLL generates high-speed clocks from 12 MHz external source.
- External memory interface (EMI) to off-chip memory-mapped devices.
- AMBA AHB system bus and APB peripheral bus.
- I^2C interface for non-volatile configuration
- Audio interfaces:
  - 4 I^2S stereo inputs supporting rates to 24-bit, 96kHz
  - 4 I^2S stereo outputs supporting rates to 24-bit, 192kHz
  - I^2S input/output configurable for AC'97 operation
  - IEC-958 (S/PDIF) input and output supporting 32kHz, 44.1kHz, 48kHz, and 96kHz
- 16-bit timer.
- Reset/clock/power management.
- Decoder controls the selection of on-chip slave blocks.
- Arbiter allows for multi-master capability of the device.
- Programmable interrupt controller (PIC) provides capability to prioritize and mask interrupts.
- Test/debug block for software development support.
- Embedded ICE/JTAG for ARM7TDMI core testing.
- Interrupt controller (IC).
- Power control.

Goals

The USS2827 is being defined as a standard product for Agere that can be used in several different application areas:

- A simple USB 2.0 device controller used to provide the USB interface and protocol handling for a client device where another processor is present.
- As the main processor in a USB client device. In this case, the processor in the USS2827 is used to run other system code in addition to the USB protocol stack.
- A USB 2.0 dial-up V.92 modem. The device has a simplified AC '97 interface that can be used to connect a low-cost SV92A3/CSP1035A soft modem chip set.

Two versions of the device are planned. A low-cost version in a 48-pin TQFP package without an external memory interface will handle simple device controller and modem operation using only the on-chip ROM and RAM. For applications that required additional memory or customer-developed application code, a 100-pin device with a 16-bit wide memory bus will be offerred at a premium price. The 100-pin device will also be used by Agere as a development vehicle for future ROM codes for the on-chip memory.

System Architecture

Figure 1 shows a block diagram of the USS2827 Device Controller. The device is based on an ARM7TDMS core and uses an AHB bus for the high-speed memories and peripherals. One of the design guidelines for the device is use single-clock synchronous logic. The AHB was choosen over an ASB bus for this reason. Low-speed peripherals are connected via an APB bus.

The sub-sections following the block diagram describe the various interfaces on the USS2827 and the major internal blocks of the device.

Interfaces

The following subsections describe the various interfaces on the USS2827. All interfaces except the external memory interface are present on the 48-pin version of the device.

ARM Test/Debug

This is the standard 5-wire JTAG interface used by the ARM development tools for loading and debugging software. This interface can also be used for loading production tests.

USB 2.0 Interface

The USB interface is the two wire differential interface (D-plus and D-minus) plus dedicated VDD and VSS pins.

EEPROM Interface

The EEPROM interface is a two wire I2C bus. Typically, the serial EEPROM is used to store small amounts of configuration information such as ID's, serial numbers, etc.

Crystal Interface

The USS2827 uses an inexpensive external 12 MHz crystal. This interface includes the two crystal connections (CKI, CKI2) as well as dedicated VDD and VSS pins.

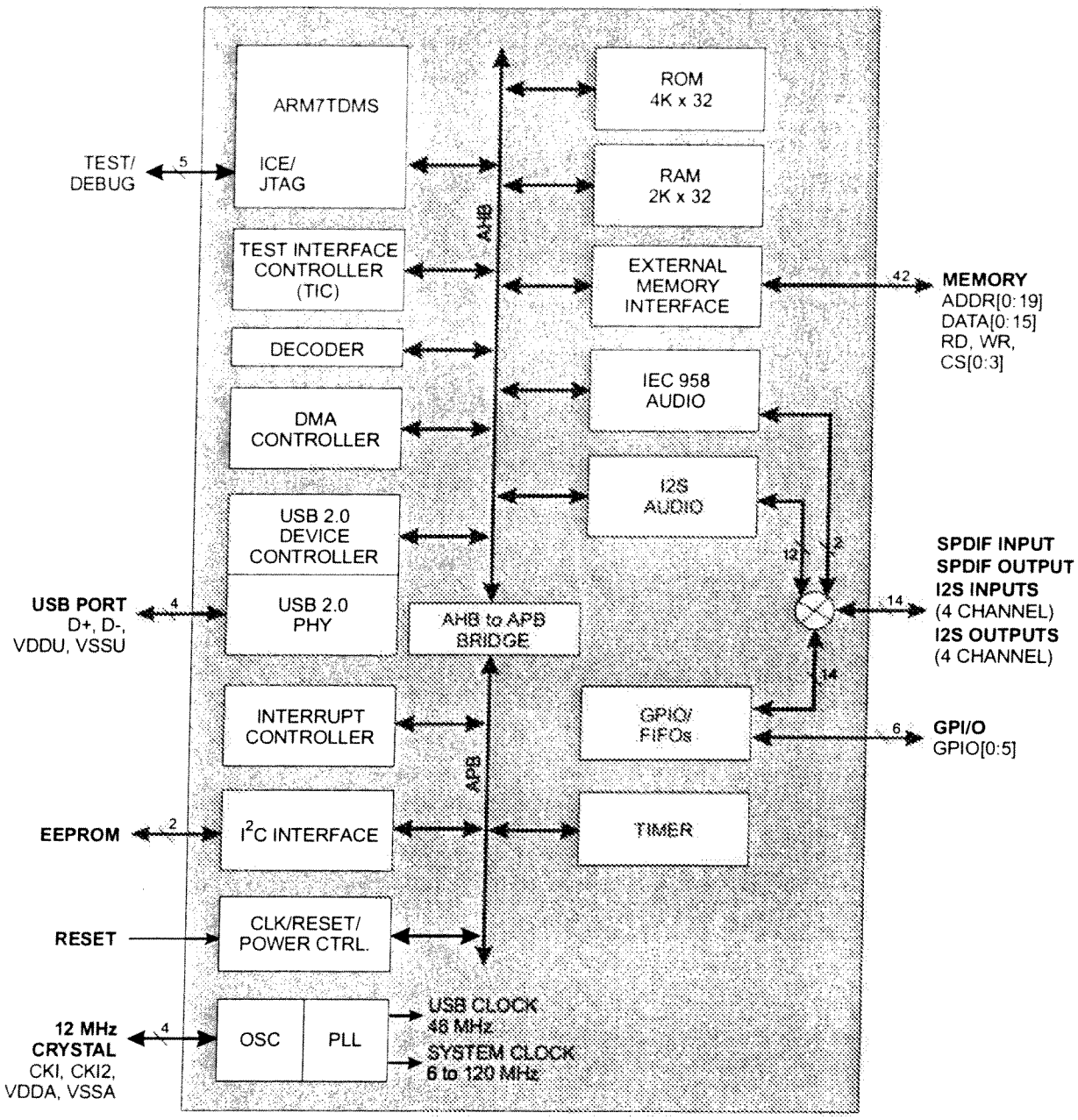


Figure 1. USS2827 Block Diagram.

General Purpose I/O and FIFO's

The GPIO and FIFO interfaces are actually two separate interfaces multiplexed together in order to reduce pin count. When the 2827 is used as a simple device controller, an external processor connects to the GPIO/FIFO interface in order to effeciently pass data over an 8-bit bus. In other applications, the port can be configured as general-purpose I/O's for connecting to external hardware.

I^2S Audio Interface

The USS2827 will support 8 channels of audio input and 8 channels of audio output on I2S interfaces (organized as 4 stereo inputs and 4 stereo outputs). The USS2827 operates as the master for all channels.

The input channels will support rates to 96 KHz and resolution to 24 bits. It is assumed that the input channels will all be configured for the same sample rate and resolution so that the SCK and WS signals can be common across the 8 input channels.

The output channels will support rates to 192 KHz and resolution to 24 bits. It is assumed that the output channels will all be configured for the same sample rate and resolution so that the SCK and WS signals can be common across the 8 output channels.

Note that this does leave the option of configuring the input and outputs at separate rates and resolutions if the application requires.

This interface can optionally be configured as two AC '97 (host) channels with the required capabilities to allow the connection of typical AC '97 audio and modem codecs. The interface should work with Agere's CSP1037D, Scorpio, SV92A2, and SV92A3 AC '97 soft modem devices (assume that the modem device is in secondary mode and the USS2827 provides the required clocks).

IEC 958 Audio Interface

The USS2827 has a single IEC 958 (aka S/PDIF) input and a single output capable of supporting 32kHz, 44.1kHz, 48kHz, and 96kHz data.

Block Definitions

The following sections describe the major blocks in the USS2827 device.

ARM7TDMS Core

The ARM7TDMS core will run at clock speeds up to 120 MHz and from the on-chip memory will yield 60 MIPs of performance. A JTAG interface is provided for connecting to the ARM development tools.

On-Chip ROM and RAM

There is 4Kx32 ROM and 2Kx32 RAM on chip accessible with zero wait states. With the 48-pin device, this is the only memory available to the ARM core.

External Memory Interface

The external memory interface is available only on the 100-pin package. This is a 16-bit wide memory bus with 20 address lines. There are four chip selects available to select external Flash ROM, RAM or other memory devices. The starting memory address and length for each device select strobe is programmable as are wait states. This allows the use of mixed on-chip and external memories.

Test Interface Controller (TIC)

A standard test interface controller is available to the ARM core to assist with production testing of the device.

Programmable Timer

A programmable timer is available to the ARM7 to enable the use of real-time OS's and for other use. The timer is programmable in increments of the 12 MHz clock period.

USB 2.0 PHY

The USB 2.0 PHY used on the USS2827 is similar to the USS2X1 standalone 2.0 phy device. The main difference is the process technology. In order to allow prototyping of the USS2827 in FPGA using an external USS2X1 phy device, the internal architecture and interface to the 2.0 Phy should mimic the USS2X1.

USB 2.0 Device Controller

The actual USB 2.0 device controller block used on the USS2827 has yet to be determined. There are several sources for standard USB 2.0 device controllers that can be used with the USS2X1 phy and it is assumed that we will re-use an available block rather than create a new one.

Programmable Interrupt Controller

The programmable interrupt controller will consolidate the various interrupt sources from within the USS2827 and allow them to be independently enabled by the ARM core.

I^2C Interface

The Inter Integration Circuit (I^2C) interface is a two-wire bi-directional serial bus that is capable of providing simple and efficient communication between devices. A single industry-standard EEPROM device will be interfaced to OCM through I^2C.

I^2C features supported in this design:

- Uses the AMBA APB protocol (ver.2.0)
- Uses I^2C bus specification (ver.2.1)
- Two data rates supported, 100Kbps and 400Kbps
- Single Master operation supporting multiple slave devices
- Programmable for normal or extended addressing (7-bit or 10-bit).
- Transfer status interrupts and flags

The I^2C interface module proposed for OCM features both an AMBA APB and an I^2C interface. The APB ports interface the I^2C module to an internal SoC APB bus. External devices that are connected to an I^2C bus can be interfaced to the module through the two bi-directional I^2C ports.

Standard I^2C features **not supported** in this design:

- High speed data rate, 3.4Mbps
- Multiple Master operation
- Bus Arbitration
- Clock Synchronization

Crystal Interface

An external 12 MHz crystal provides the clock source for the device with an internal PLL to generate the required 48 MHz clock for the USB interface. Note that the PLL is a simple "x4" block. The other rates are generated by dividing the 48 MHz clock.

Clock and Power Control

An on-chip power-up reset generator works in conjunction with an external RESET signal to control the internal reset of the device. The ARM clock for the ARM core can be selected as the 48 MHz clock or lower rates or 6, 12 or 24 MHz which are generated by enabling clock dividers.

At power-up, the crystal interface is enabled and the PLL is disabled. The ARM7 core runs at the 12 MHz crystal rate and boots from on-chip ROM.

There are independent clocks for most peripherals on the USS2827, allowing blocks not required in any specific mode to be disabled in order to minimize power dissipation.

I^2S Audio Interface

The I2S audio interface connects to the ARM AHB bus and provides 4 channels of stereo input and 4 channels of stereo output that are independently configurable. Sufficient hardware fifo's are provided for both inputs and outputs to ensure that data streams are not corrupted due to ARM software latencies.

This interface can optionally be configured as two AC '97 (host) channels with the required capabilities to allow the connection of typical AC '97 audio and modem codecs.

IEC 958 Audio Interface

The ISC 958 audio interface connects to the ARM AHB bus and provides a single input and output. Sufficient hardware fifo's are provided for both input and output to ensure that data streams are not corrupted due to ARM software latencies.

Exh. 3

-----Original Message-----
From: Harrington, John Timothy (John)
Sent: Wednesday, May 07, 2003 10:24 PM
To: Harrington, John Timothy (John); Atre, Madhusudan V (Madhu)
Cc: Swearingen, Stanley A, Jr (Stan); Rai, Surinder Singh (Surinder); Fields, Jonathan A (Jon); Staves, Sherre M (Sherre); Thompson, David W (Dave)

Subject: RE: Support "proposal" from IDC

Madhu,

We would like to have both programs [redacted] and USS2827) be supported by your team(s) in terms of the RTL integration and verification activities. Mapping in the timeframe in which your folks are freeing up, we would like to propose the following resource ramp:

	1-3weeks(ASAP?)	6/15	7/1
[redacted]	3 designers	4 designers	4 designers (represents total design HDCT)
USS2827	1 designer	2 designers	4 designers (represents total design HDCT)

This plan would require an additional HDCT hire starting July. Let me know what type of additional information you need to begin that process.

My understanding is that Prasad will be visiting soon, it would be beneficial for all of us (Prasad, Dave, Sherre, JTH) to sit down and review these plans - please let me know the dates he will be in the US. We want to get started with the information flow quickly. Thanks.

(PS - also attached is the current view system requirement document for the USS2827 - it is in MRI if you have access to that system)

John Harrington
Agere Systems
jtharrington@agere.com
610-712-2421 (phone)
610-712-4277 (fax)
1110 American Parkway NE Rm.12B-264
Allentown, PA 18109-9138

-----Original Message-----
From: Harrington, John Timothy (John)
Sent: Monday, May 05, 2003 7:55 AM
To: Atre, Madhusudan V (Madhu)
Cc: Swearingen, Stanley A, Jr (Stan); Rai, Surinder Singh (Surinder);
Fields, Jonathan A (Jon); Harrington, John Timothy (John)
Subject: RE: Support "proposal" from IDC

Madhu,

These plans need to be reconciled with Stan - but wanted to give you a heads up in our current thinking. Answers to questions 5 and 6:

5) - The intent would be to keep some continuum of design programs to keep those 9 people busy on an ongoing basis - do not know what those programs will be after this round.

6) - The IP HDCTs would be in addition to the design HDCTs. The plan was to target the new fiscal year for these reources, assuming the plan gets approved.

My plan is to close with Stan and PL heads to review this proposal and associated costs to implement them. I will keep you posted. We should defintely target using the 4HDCT that would be freeing up soon for one of the two near term programs.

John Harrington
Agere Systems
jtharrington@agere.com
610-712-2421 (phone)
610-712-4277 (fax)
1110 American Parkway NE Rm 12B-264
Allentown, PA 18109-9138

-----Original Message-----
From: Harrington, John Timothy (John)
Sent: Friday, May 02, 2003 5:53 PM
To: Atre, Madhusudan V (Madhu)
Cc: Harrington, John Timothy (John); Swearingen, Stanley A, Jr (Stan); Rai, Surinder Singh (Surinder)
Subject: Support "proposal" from IDC

Madhu,

Please see attached XL spreadsheets for an estimate of near term activities, plus a view of FY'04 plans to continue with design and add IP activities. Let me know when Prasad is in town to review. Thanks.

(Surinder - we will have to compare notes on IDC near term availability versus the other 3rd party options being pursued. If IDC can cover, it presents several choices; if Madhu cannot ramp fast enough, it pushes the decision towards 3rd party).

John Harrington
Agere Systems
jtharrington@agere.com
610-712-2421 (phone)
610-712-4277 (fax)
1110 American Parkway NE Rm 12B-264
Allentown, PA 18109-9138

-----Original Message-----
From: Atre, Madhusudan V (Madhu)
Sent: Friday, May 02, 2003 3:10 AM
To: Harrington, John Timothy (John)
Subject: RE: Loaded Cost at IDC

John: Prasad is likely to visit LVCC in a week or so. If you could send inputs, I can discuss w/ him prior to his visit so that he can come w/ concrete plans to discuss w/ you and others.
Regards, Madhu.

-----Original Message-----
From: Ramesh Sirsi [mailto:rsirsi@umsi-us.com]
Sent: Thursday, May 15, 2003 3:03 PM
To: Perlove, Kathi M (Kathi); Thompson, David W (Dave)
Cc: Billowitch, William David (Bill)
Subject: Re: IP SOW and updated SRD

Kathi,

I will follow up with the design group and update the project schedule.
I have two questions on the SRD document.

1.Sec 2.1 IP requirements - Will this be a separate document ? 2. Sec 3.9 Earned Value Analysis - I need a short tutorial on this.

Thanks

Ramesh

Dave,

I took a quick look at the updated SRD document and did not see any changes to the functional block diagram on page 4 w.r.t to last revision I received from you in April. Are there any changes that relates to design tasks?

Thanks

Ramesh

"Perlove, Kathi M (Kathi)" wrote:

>> Ramesh,
>> Attached please find the updated SRD and the IP SOW from Bill
>> Billowitch. Please review the checkpoints required in the SOW and add
>> to your schedule where appropriate. Let me know if you have any
>> questions, Regards,
>>
>> Kathi
>> <<IP-SOW.doc>> <<USS2827_SRD_05132003.pdf>>
>>
>>

>> Name: IP-SOW.doc
>> IP-SOW.doc Type: WINWORD File (application/msword)
>> Encoding: base64
>>
>> Name: USS2827_SRD_05132003.pdf
>> USS2827_SRD_05132003.pdf Type: Acrobat (application/pdf)
>> Encoding: base64 << File: Card for Ramesh

Sirsi >>
<<IP-Requirements-USB2.0-Device.xls>>

Dave,

I have been discussing with the design group regarding man power estimates required for FPGA targeting. They sent me the following as basis for their effort estimation. Please let me know if this assumption is o.k. or Agere will implement some of the steps internally. I would also like to get details of FPGA target board:

Incremental effort required for FPGA involves the following steps

- RTL Conversion for FPGA
- Synthesis
- P&R
- Timing Verification
- Bit Stream

Ramesh

Ramesh Sirsi <rsirsi@umsi-us.com

Dave,

Design team reviewed the latest version of SRD and noted following updates:

-----Original Message-----
From: Ramesh Sirsi [mailto:rsirsi@umsi-us.com]
Sent: Tuesday, May 20, 2003 5:00 PM
To: Dave Thompson
Cc: Perlove, Kathi M (Kathi); Surinder Rai; William David Billowitch
Subject: FPGA

Dave,

I have been discussing with the design group regarding man power estimates required for FPGA targeting. They sent me the following as basis for their effort estimation. Please let me know if this assumption is o.k. or Agere will implement some of the steps internally. I would also like to get details of FPGA target board:

Incremental effort required for FPGA involves the following steps

- RTL Conversion for FPGA
- Synthesis
- P&R
- Timing Verification
- Bit Stream

Ramesh

Surinder:

Attached is the DesignWare license agreement. In summary:
a. We paid for the DesignWare fees, IDC has access to this tool
b. The USB 2.0 Device Controller is available as part of this fee
c. [redacted] are indicated in this agreement.
d. GateLevel versions of the USB device controller CAN be sublicensed
e. RTL is available for a [redacted] fee only if we need to have it (which I do not believe is necessary)
f. This core is proven in silicon.

Commentary:
With IDC doing the integration and verification, my recommendation is that

-----Original Message-----
From: Dave Thompson [mailto:davethompson@agere.com]
Sent: Friday, May 30, 2003 1:37 PM
To: Hal Barbour
Subject: Re: Sorry, forgot to make the attachment

Hal,

whose usb2 phy are you using in your demo?

Dave

>> Hal Barbour wrote:
>>
>> Dear Agere team,
>>
>>
>>
>> We appreciate the opportunity to conference with you today at 1 PM

regarding your

>> requirement for a USB 2.0 core. We have put together a few slides that we

plan to

>> go over in the call. The PowerPoint presentation is attached.
>>
>>
>>
>> Looking forward to meeting with you at 1 PM today.
>>
>>
>>
>> Regards,
>>
>> *
>>
>> Hal Barbour
>>
>>
>>
>> Toll Free: 888-476-6131
>>

-----Original Message-----
From: Steven ERICKSON [mailto:serickson@creativelabs.com]
Sent: Monday, June 02, 2003 9:30 PM
To: Ondrasek, Daniel Denys (Dan)
Subject: Re: Quote

Dan,

Thanks. I will get back to you next week on the development boards. Can you also give me an
updated schedule for this?

Steve Erickson
serickson@creativelabs.com
408 546 6945

"McGowan, Rosemary T (Rosemary)" <rtmcgowan@agere.com>

To: <serickson@creativelabs.com>
cc: "Ondrasek, Daniel Denys (Dan)" <ondrasek@agere.com>
Subject: Quote

06/02/2003 11:33 AM

Hello,

Please see attached quote:

Please contact Dan Ondrasek with any questions.

Regards,

Rose McGowan
Inside Sales Manager
Agere Systems Inc

(978-691-3352
7 978-691-3353
* rtmcgowan@agere.com

Attachment(s) removed in mail thread by Steven ERICKSON on 2 Jun 2003 9:27:57 PM :
Creative quote 6 2.doc

FYI --

Kathi

-----Original Message-----
From: Devine, Daniel J (Dan)
Sent: Monday, June 09, 2003 3:34 PM
To: Thompson, David W (Dave)
Subject: FW: [Fwd: Re: USB2 phy on com2H?]

Dave;

May we get a die size estimate in com2H?

Dan

-----Original Message-----
From: Hoke, Samuel Andrew (Sam)
Sent: Monday, June 09, 2003 3:21 PM
To: Devine, Daniel J (Dan); Rai, Surinder Singh (Surinder)
Subject: [Fwd: Re: USB2 phy on com2H?]

FYI. Looks like we'll have a usb2 phy in com2h later this year.

- Sam

-----Original Message-----
From: dave thompson [mailto:davethompson@agere.com]
Sent: Thursday, June 12, 2003 2:01 PM
To: Perlove, Kathi M (Kathi)
Cc: Devine, Daniel J (Dan); Hoke, Samuel Andrew (Sam)
Subject: Re: USS2827 Com1H or Com2?

Kathi,

I should be free at 3pm...

Dave

> "Perlove, Kathi M (Kathi)" wrote:
>
> Dan,
> Dave and I talked Monday and I thought we were proceeding with Com1H. I heard
> from Surinder that there was a possibility of moving this to Com2? I just want to
> keep us all on the same page.
>
> In fact, if Dave is in town today, can we have a quick call to discuss how we want
> to proceed with the audio blocks? Bill Billowitch is in meetings all day but he
> left me a message with his clear preference as [redacted] due to his desire to use other
> blocks in their library for future Agere products. Again, I want to make sure we
> are all in sync too.
>
> I am available any time except 1:30 - 2:30pm. Can we meet at 3pm today?
> Thanks
>
> Kathi

OUCH!!!!

-----Original Message-----
From: Ondrasek, Daniel Denys (Dan)
Sent: Thursday, June 12, 2003 7:14 PM
To: Devine, Daniel J (Dan)
Subject: FW: FW: USS2827

FYI

-----Original Message-----
From: Steven ERICKSON [mailto:serickson@creativelabs.com]
Sent: Thursday, June 12, 2003 2:26 PM
To: Ondrasek, Daniel Denys (Dan)
Subject: Re: FW: USS2827

Dan,

To follow up on the RAM size we will be more comfortable with 64k.

Steve Erickson
serickson@creativelabs.com
408 546 6945

Steven ERICKSON
06/11/2003 01:06 PM

To: "Ondrasek, Daniel Denys (Dan)" <ondrasek@agere.com>
cc:
Subject: Re: FW: USS2827(Document link: Steven ERICKSON)

Dan,

Here is some more confidential information. I am still trying to get the total RAM requirement.

What is the Cirrus Logic part number?
EP7309

What is the RAM requirement needed?
Right now the entire 48k of internal RAM is used for firmware code and for data buffers. We will

-----Original Message-----
From: Agnello, John Charles (John)
Sent: Friday, June 13, 2003 11:07 AM
To: Buella, Querubin, Jr (Querubin)
Subject: FW: CPU & Allegro Specs

Querubin, here is the customer's spec on what they are looking for in a processor with USB. Does our new device look anything like this?

Best Regards,

John Agnello
Agere Systems
Sales Engineer
805-499-8681 (office)
805-208-3988 (cell)
805-376-8481 (fax)
jagnello@agere.com

Kathi,

I am attaching revised proposal for development of the two audio cores. Development charges have remained the same as in the previous proposal. Development schedule has increased incrementally reflecting on additional effort required to comply with SoW. I have not included activities relating SoC integration and verification. We will submit a detailed mpp schedule after we complete defining the core blocks. I am waiting to receive IEC 958 standard document from Dave to complete this exercise.

Please let me know if you need any additional inputs from me. Look forward to hearing from you.

Regards,

Ramesh

Ramesh Sirsi <rsirsi@umsi-us.com>
United Micro Solutions Inc.

Kathi,

I missed identifying two additional tools we need to access from your design facility in Bangalore. I have updated this requirement in the attached proposal.

Thanks

Ramesh

Ramesh Sirsi wrote:

>> Kathi,
>>
>> I am attaching revised proposal for development of the two audio cores.
>> Development charges have remained the same as in the previous proposal.
>> Development schedule has increased incrementally reflecting on
>> additional effort required to comply with SoW. I have not included
>> activities relating SoC integration and verification. We will submit a
>> detailed mpp schedule after we complete defining the core blocks. I am
>> waiting to receive IEC 958 standard document from Dave to complete this
>> exercise.
>>
>> Please let me know if you need any additional inputs from me. Look
>> forward to hearing from you.
>>
>> Regards,
>>
>> Ramesh
>>
>> ----------
>> Name: IEC958 Proposal.pdf
>> IEC958 Proposal.pdf Type: Acrobat (application/pdf)
>> Encoding: base64

Ramesh Sirsi <rsirsi@umsi-us.com>
United Micro Solutions Inc.

Folks;

We need to get together to determine the impact of a 64K RAM in the USS2827

per the email below. Please email me a few dates and times you are available, sooner rather than later.

Thanks;
Dan

-----Original Message-----
From: Ondrasek, Daniel Denys (Dan)
Sent: Thursday, June 12, 2003 7:14 PM
To: Devine, Daniel J (Dan)
Subject: FW: FW: USS2827

FYI

-----Original Message-----
From: Steven ERICKSON [mailto:serickson@creativelabs.com]
Sent: Thursday, June 12, 2003 2:26 PM
To: Ondrasek, Daniel Denys (Dan)
Subject: Re: FW: USS2827

Dan,

To follow up on the RAM size we will be more comfortable with 64k.

Steve Erickson
serickson@creativelabs.com
408 546 6945

Steven ERICKSON

06/11/2003 01:06 PM

To: "Ondrasek, Daniel Denys (Dan)" <ondrasek@agere.com>
cc:
Subject: Re: FW: USS2827(Document link: Steven ERICKSON)

Dan,

Here is some more confidential information. I am still trying to get the

-----Original Message-----
From: Steven ERICKSON [mailto:serickson@creativelabs.com]
Sent: Monday, June 16, 2003 9:26 AM
To: Ondrasek, Daniel Denys (Dan)
Subject: Re: 2827 need clarification

Dan,

I believe this should be Bytes.

Steve Erickson
serickson@creativelabs.com
408 546 6945

"Ondrasek, Daniel Denys (Dan)" <ondrasek@agere.com>
06/16/2003 08:44 AM

To: "Steve Erickson (E-mail)" <serickson@creative.com>
cc:
Subject: 2827 need clarification

Steve-

Good morning...hope the weekend was good. We are looking for a clarification.
Can you confirm that it is 64K bytes(by 8) or 64K words(by 16).

Thanks for your help.
Regards,
Dan

Dan Ondrasek
Agere Systems
(408) 980-3843 office
(408) 838-6436 cell
ondrasek@agere.com

Dave,
Looks like we are covered by Bill.

Kathi

Exh. 4

-------- Original Message --------
Subject: Queries w.r.t USS2827/SV92A3 devices
Date: Tue, 27 May 2003 08:53:21 -0400
From:A V S S, Prasad (Prasad) <avssp@agere.com>
To: Staves, Sherre M (Sherre) <staves@agere.com>, Thompson, David W (Dave) <davethompson@agere.com>, Hoke, Samuel Andrew (Sam) <shoke@agere.com>
CC: Harrington, John Timothy (John) <jtharrington@agere.com>, A V S S, Prasad (Prasad) <avssp@agere.com>

Dave,Sherre,

Following are some of the queries I have w.r.t these two devices. I also
copied Sam on this mail. If he is not the right person, please do forward
this mail to to the concerned people.
We are meeting on Wednesday at 10.00 am to continue our discussions. We also
need to discuss about the design flow and the hand-off between the Physical
Designer and the team @ IDC. Is PUNT to be used ?

Rgds
Prasad

==========
=
Queries with respect to the USS2827 device controller

--

1. What is the frequency of operation of the CPU and the AHB bus ?
2. What is the technology to be used ? [Understand that we will be using 0.2
u technology - COM1H]
3. Why AHB interface for the I2S interface ? [Is it because of the multiple
channels]
4. We need to have wrappers for ROM and RAMs in order to make them AHB
compatiable. Is this assumption correct or we are likely to have some kind
of AHB compatiable memory controller?
5. Are the sizes of the RAM/ROM same for both 48-pin and 100-pin devices ?
6. Does the USB device [from synopsys] have a behavioural model for checking
the behaviour in the Verification environment ?
7. What is the role of TIC?
8. Any test modes planned ?

9. The GPIO/FIFO is connected to the I2S controller. In the "simple device
controller" mode, the data written into the FIFOs is not accessible to other
devices, on-chip?
10. What DFT methodology is going to be used ?
11. What is the memory map of on-chip RAM/on-chip ROM/EMI space ?
12. What kind of power control is planned for this device ?
13. Any specific requirements for the I/O buffers ?
14. Does UMSI plan to deliver the driver/monitors for the IP, they are developing ?
15. Do we have driver/monitors for the existing inhouse IPs ?
16. What is the configuration of DMA? What all peripherals can use the DMA
channels? Is it only for on-chip ?

Queries w.r.t the SV92A3 device:
---

1. What is the interface between the AC-97 and Codec Logic ?
2. What is the configuration bus, to be used, for configuring the device ?
3. Any additional test modes ?
4. Does the codes still have all the FIFO interfaces as they are in the existing architecture ?
5. What about the interrupt interface from the Codec ? (It was going to the
DSP1600)
6. Any power down options ?
7. What is the frequency of operation ?
8. Technology ? [Guess it is 0.2 u - COM1H]
9. Any specific requirements for the I/O buffers ?

==========

Exh. 5

AGERE SYSTEMS INVENTION SUBMISSION

This invention submission is being provided to an attorney in order to determine how to protect intellectual property and to facilitate efforts to acquire appropriate protection. Distribution of this invention submission shall be limited to attorneys and persons acting on behalf of Agere to facilitate making such determinations.

Name(s) of Submitters	Telephone No:	Loc/Room	SBU/Org. Title:	HR ID:	E-Mail Address
Daniel Devine	610-712-6802	12B-284	CCD-Wired	7499627	dandevine@agere.com

IP LAW USE
Submission No: 124809
Date Received: July 11, 2003
Attorney: Robert P. Marley

TITLE: ARM7 Processor based USB 2.0 Device Controller

Important Notes: (1) Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple. (2) Have any of the above submitter(s) discussed this invention with, or provided an invention submission disclosing this invention to, an attorney other than the recipient of this invention submission? ____YES ____NO

1. Describe the problem your invention solves:

An ARM7 Processor based USB 2.0 device controller provides a flexible platform for computer peripheral manufacturers to quickly and cost-effectively implement USB 2.0 PC interconnect technology into their products.

2. Based on information of which you are already aware, describe:

(i) previous attempts to solve the problem your invention solves:

previous attempts with on-board processors proved to be under-powered. With an ARM7 processor on-board, it is now possible to eliminate the current processor in the PC peripheral.

(ii) the disadvantages of the previous attempts:

Lack of MIPs (millions of instructions per second) in previous attempts meant that the USB 2.0 device could only provide the USB 2.0 functionality, but not the functionality of the peripheral, be it a camera, scanner, printer, etc.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

By integrating a powerful ARM7 processor this invention solves the problem by off-loading the existing peripheral processor to the point that processor can be eliminated from the architecture resulting in less cost and smaller form factor.

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

The USS2828 USB 2.0 Device controller is a product targeted at the rapidly growing market for USB 2.0 Peripherals. It is estimated the silicon market size is $487M, of which Agere could capture 13% share, or at least $61M over a 3 year period.

The USS2828 shall:

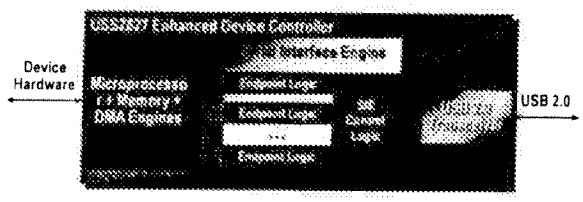
- Provide customers a complete, certified USB 2.0 peripheral solution including software and a powerful microprocessor.
- Be a lead for USB 2.0 device IP development for Agere Integrated ASICs for:
  - Oak Technology ASIC
  - Hermes 3 (802.11 MAC)
  - Two-Wire ASIC

- The processor in the USS2828 shall provide additional MIPs over and above that required for fundamental USB 2.0 traffic processing.
- The additional MIPs shall provide customers with the opportunity to remove their existing peripheral microprocessor, thereby eliminating cost and form factor.
- The USS2828 will be used as a USB 2.0 soft modem device with the potential to sell 1 million units per year.
- Competitive advantage shall be provided by Agere's superior software algorithm capabilities which will allow for higher (value) pricing.

The USS2828 shall be manufactured in the lowest available cost technology including up-front mask costs, recurring costs, and risk (as it relates to TTM - Time to Market)

agere

USS2827 Block Diagram



5. Advantages of your invent

Improved Cost and form factor (size) can be achieved via the use of this type of device. The integration of a powerful ARM7 processor off-loads the existing peripheral processor to the point that the existing peripheral processor can be eliminated from the architecture.

6. Explain how use of your invention would be detected:

A de-capping of a USB 2 peripheral device would show an ARM7 block on the die, along with circuitry to a USB 2.0 connection.

Submitter(s) signature(s) and date:

_____ _____ **date**

_____ _____ **date**

_____ _____

This invention submission has been read and understood by the following two witnesses:

_____ _____ **date**

_____ _____ **date**

ATTORNEY-CLIENT PRIVILEGED DOCUMENT

*** Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc ***

Exh. 6

agere systems

Kyshon J. Rivers
Outside Counsel
Coordinator
Intellectual Property Law

Connell Corporate Center IV
4 Connell Drive
Room 4U-533D
Berkeley Heights, NJ 07922
Tel: 610-712-8514
Fax: 610-712-8544
krivers@agere.com
www.agere.com

October 15, 2003

Kevin Mason, Esq.
Ryan, Mason & Lewis, LLP
1300 Post Road
Suite 205
Fairfield, CT 06430

1150-1212

Re: **IDS No.:** 124809 **(CLASS III)**

Managing Attorney	**Telephone No.**	**Fax No.**
Bob Marley	(610) 712-8516	(610) 712-8544
Secretary	**Telephone No.**	
Judith Williams-Matthew	(610) 712-8525	

Dear Kevin:

The above-referenced patent submission enclosed with this letter should be filed by **January 15, 2004**, in accordance with Agere's general instructions for Outside Counsel, previously furnished to you. If, for any reason, you cannot meet the filing date requested, you MUST notify the Managing Attorney (MA) and me, VIA FACSIMILE, as soon as possible.

After the final claims have been drafted and you are therefore in a position to identify the inventors, please send "Request for Case Name/Number" (ATTACHMENT G), VIA FACSIMILE, to me at (610) 712-8544.

Unless the MA has otherwise agreed, our instructions are that a copy of the proposed application is to be sent to the MA prior to execution of the Declaration and Assignment; likewise, all other substantive papers such as amendments, appeal briefs and the like are to be sent to the MA prior to filing. Please note, however, that the MA may not be in a position to review the application or other papers prior to filing, or may choose to conduct only a quality control review either now or at a later time. Accordingly, the ultimate responsibility for the timely filing as well as the quality and contents of the papers of this application and any resulting patent rests with you. **If you do not receive specific instructions from the MA within eight (8) business days from the date that the application or any subsequent papers were submitted to the MA, you are authorized and directed to transmit same directly to the USPTO.**

This application will not be foreign filed.

If, during the prosecution of an application, you believe that a CPA/CIP, Divisional, Appeal, etc. should be filed, your advice should be presented to the Managing Attorney for concurrence, prior to commencement of any work.

Very truly yours,

Kyshon

Kyshon J. Rivers

Enc.

Exh. 7

Kevin Mason

From: Devine, Daniel J (Dan) [dandevine@agere.com]
Sent: Monday, January 12, 2004 2:22 PM
To: kmm@rml-law.com
Subject: MRD & SRD

Hi Kevin;

Nice meeting you today. As requested please find the SRD and MRD for the USS2827 device.

Please let me know if there is anything else you might need.

Thanks;

Dan

<<USS2827___2828_StdProductMRDAug2003Rev_0[1].95.doc>> <<USS2828_SRD_12162003.doc>>

Ex. 8

Kevin Mason

From: Devine, Daniel J (Dan) [dandevine@agere.com]
Sent: Tuesday, February 03, 2004 3:43 PM
To: kmm@rml-law.com
Subject: Patent Form & Block Diagram

<<USB2devicepatentform.doc>> <<USS2828PatentSlides.ppt>>

Hi Kevin;

Please let me know what else you need. Just an FYI, we were in the process of created two versions, one for a customer with lots of audio capability (the USS2827) and one for use in simpler peripherals and as a USB 2 soft modem (the USS2828).

Thanks;
Dan

Kevin Mason

Exh. 9

From: Kevin M. Mason [kmm@rml-law.com]
Sent: Thursday, February 05, 2004 5:28 PM
To: Devine, Daniel J (Dan)
Subject: Agere Patent Matter 124809


1150-1212.app.doc (79 KB) 1150-1212.FIGS.doc (113 KB)

Hi Dan:

I attach a draft of the above application for your review. Please carefully review the enclosed application to ensure that it is clear and complete, sets forth the best mode contemplated by each inventor for carrying out the invention, and contains a sufficient disclosure to enable a person of ordinary skill in the art to make and use the invention. There is some additional work to be done on my end. If possible, I'd like to discuss your comments early next week, so that I can turn around another (hopefully, final) draft before I leave for vacation on 2/12.

Please let me know if you have any questions or comments.
Best regards,
Kevin

--
Kevin M. Mason
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06430
(203) 255-6558 (voice)
(203) 255-6570 (fax)

Exh. 9

Subject: RE: Agere Patent Matter 124809
From: "Devine, Daniel J (Dan)" <dandevine@agere.com>
Date: Mon, 23 Feb 2004 09:33:29 -0500
To: "Kevin M. Mason" <kmm@rml-law.com>

Hi Kevin;

I thought I had responded to you via email on this.

The draft is fine, go with it.

Thanks;
Dan

-----Original Message-----
From: Kevin M. Mason [mailto:kmm@rml-law.com]
Sent: Monday, February 23, 2004 8:02 AM
To: Devine, Daniel J (Dan)
Subject: Re: Agere Patent Matter 124809

Hi Dan:
How is your review coming along on the patent draft? We'd really like to get the application filed this week (which means we need to get the application to the Managing Attorney for review as soon as possible).
Regards, Kevin

Kevin M. Mason wrote:

> Hi Dan:
> I attach a draft of the above application for your review. Please carefully review the enclosed application to ensure that it is clear and complete, sets forth the best mode contemplated by each inventor for carrying out the invention, and contains a sufficient disclosure to enable a person of ordinary skill in the art to make and use the invention. There is some additional work to be done on my end. If possible, I'd like to discuss your comments early next week, so that I
>
> can turn around another (hopefully, final) draft before I leave for vacation on 2/12.
>
> Please let me know if you have any questions or comments. Best regards, Kevin

Exh 9

Subject: RE: Devine 2
From: "Devine, Daniel J (Dan)" <dandevine@agere.com>
Date: Mon, 23 Feb 2004 21:42:33 -0500
To: "Kevin M. Mason" <kmm@rml-law.com>

Kevin;

Thanks for your efforts on this.

It looks good.

Dan

-----Original Message-----
From: Kevin M. Mason [mailto:kmm@rml-law.com]
Sent: Monday, February 23, 2004 5:38 PM
To: Devine, Daniel J (Dan); Marley, Robert P (Bob)
Subject: Devine 2

Genetlemen:
I attach a final draft of the above application for your review. Please carefully review the enclosed application to ensure that it is clear and complete, sets forth the best mode contemplated by each inventor for carrying out the invention, and contains a sufficient disclosure to enable a person of ordinary skill in the art to make and use the invention. We'd like to file this application by Friday, Feb. 27, 2004.

Please let me know if you have any questions or comments.
Best regards,
Kevin

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Kevin M. Mason
Attorney at Law
Washington, DC 20037

Exh. A

NEW MATTERS TO BE HANDLED BY CT OFFICE FOR WEEK ENDING OCTOBER 17, 2003

CLIENT	FILE NO.	TITLE	INVENTOR(S)	CLIENT ATTY	RM&L ATTY	BRIEF DESCRIPTION/ KEYWORD(S)	DISPOSITION (ACCEPTED/ RETURNED)
Agere	1150-1212	ARM7 Processor Based USB 2.0 Device Controller	D. Devine	RPM	KMM	ARM7 processor in PC controller eliminates processor in USB peripheral	Accepted

Acknowledgment:

	Initials:	Date:
Joseph B. Ryan	JBR	10/20/03
Kevin M. Mason	KMM	10/20/03
William E. Lewis	WEL	10/21/03
Wayne L. Ellenbogen	WLE	10/20/03
Robert J. Mauri	RJM	10/20/03
Michael J. Chang	MJC	10/20/03
Robert W. Griffith	RWG	10/20/03
James P. Jamiello	JPJ	10/20/03

Exh. 8

James Janniello

From: Kevin Mason
Sent: Sunday, June 14, 2009 9:03 AM
To: James Janniello
Subject: FW: New Agere Patent Matter 124809

From my email archive...

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Kevin M. Mason
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6558 (voice)
(203) 255-6570 (fax)

-----Original Message-----
From: Kevin M. Mason [mailto:kmm@rml-law.com]
Sent: Monday, October 20, 2003 8:38 AM
To: dandevine@agere.com
Subject: New Agere Patent Matter 124809

Hi Daniel:
I am an outside patent attorney, and we will be working together on the above patent application. Agere has asked us to complete this matter by Jan. 15, 2004. We will work with this deadline, unless there are any prior plans to publish or commercialize the invention. With my current work load, I estimate that I will begin actively working on this matter in late November. Please let me know if we need to alter the deadline, or if you have any questions.
Best regards,
Kevin Mason

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Kevin M. Mason
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06430
(203) 255-6558 (voice)
(203) 255-6570 (fax)